REMARKS

The Office Action dated January 6, 2005 has been received and carefully considered. In this response, claims 1, 3, 7-9, 12, 15, 18, 21-23 and 38 have been amended, claims 24-25 have been canceled and new claims 44-54 have been added. The claims have been amended to remove reference to unnecessary "step of" language. These amendments do not alter the scope of the claims. Support for these amendments and the addition of new claims 44-54 may be found in the specification and drawings as originally filed. Entry thereof and reconsideration of the outstanding rejections in the present application is respectfully requested.

Anticipation Rejection of claims 1-8, 13, 19, 20, 36 and 37

At page 2 of the Office Action, claims 1-8, 13, 19, 20, 36 and 37 were rejected under 35 U.S.C. Section 102(e) as being anticipated by Mirov (U.S. Patent No. 6,691,215). This rejection is respectfully traversed.

Claim 1, from which claims 2-8, 13, 19 and 20 depend, recites the limitations of disabling a phase locked loop when in a first power mode. Claim 36, from which claim 37 depends, recites similar limitations. Non-limiting examples of disabling a phase locked loop (PLL), as provided by the present application, may include disabling clock signals input to a PLL or shutting off power to a PLL. *See Present Application*, p. 7, lines 12-18. With respect to these limitations, the Examiner asserts that Mirov teaches disabling a phase locked loop "by asserting PLL BYPASS signal." *Office Action*, p. 2. The Examiner also cites Figure 18 of Mirov and the passage of Mirov at col. 21, line 27 – col. 23, line 56 in reference to the additional limitations recited by dependent claims 8 and 19 with regard to disabling a PLL. *Id.*, p. 3.

The Applicants respectfully submit that, contrary to the assertions of the Office Action, Mirov fails to disclose the limitations of disabling a PLL when in a first power mode. Instead, Mirov provides that the PLL of Mirov is merely bypassed during an idle mode. As illustrated by Figure 10 of Mirov, the PLL BYPASS signal, referenced by the Examiner, is used as the select control of the multiplexer 1010. Thus, the PLL BYPASS signal controls whether the CLOCK IN SIGNAL or the output of the VCO 1004/divider 1006 is output to the clock tree 1012. However, as also illustrated by Figure 10 of Mirov and by the use of the term "bypass" in its

name, the PLL BYPASS signal does disable the operation of the PLL 904, but merely causes the CLOCK IN signal to bypass the PLL. *See Mirov*, col. 16, line 27-40 ("Alternatively, when the PLL BYPASS signal is asserted, the multiplexer 1010 passes the CLOCK IN signal to the clock tree 1012. In this mode of operation, the PLL 904 is effectively bypassed, with the CLOCK IN signal being substantially directly distributed by the clock tree 1012. Thus, since the PLL 904 is bypassed, the CLOCK OUT signal is no longer synchronized with the CLOCK IN signal. . . .) (emphasis added). Likewise, no remaining passage of Mirov discloses that the PLL BYPASS signal is used to disable a PLL.

Not only does Mirov fail to disclose that the PLL BYPASS signal disables a PLL, Mirov fails to disclose that a PLL is disabled in any manner. As noted above, the Examiner refers to the passage of Mirov at col. 21, line 27 – col. 23, line 56 in support of the Examiner's assertion that Mirov teaches "a power supply comprised of power modules and method of providing reduced power in comparison to available power to the device" and "enabling/disabling the power modules to produce desired voltage and make available the desired current on a line of different operating modes." *Office Action*, p. 3. While the Applicant agrees with the Examiner that Mirov teaches "a method of providing reduced power" in that Mirov teaches that the power modules 1904, 1906 and 1908 of a power supply 1800 can be selectively disabled to provide reduced power to the computer system 200 (*see, e.g., Mirov*, col. 22, lines 24-34 and Figure 19), the Applicant respectfully submits that Mirov provides no disclosure that the provision of a reduced amount of power disables the PLL of Mirov in any way. Mirov provides no disclosure indicating that the power supplied to the PLL is reduced and, as will be appreciated by those skilled in the art, the reduction in the total amount of power provided by the power supply 1800 to the computer system 200 does not necessarily require that the power supplied to the PLL be reduced. Moreover, even if Mirov disclosed a reduction in the power supplied to the PLL (which Mirov does not), Mirov provides no disclosure that a power reduction would disable the PLL and one of ordinary skill in the art will appreciate that a reduction in power supplied to a PLL does not necessarily disable a PLL.

Accordingly, the Applicants respectfully submit that Mirov fails to disclose at least the limitations of disabling a phase locked loop when in a first power mode as recited by claims 1 and 36. The Office Action therefore fails to establish that Mirov discloses each and every

limitation of claims 1 and 36, as well as claims 2-8, 13, 19, 20 and 37 at least by virtue of their dependency from one of claims 1 or 36. Moreover, these claims recite additional limitations that are not disclosed by Mirov. To illustrate, claim 19 recites the additional limitations of wherein disabling the phase locked loop includes shutting of power used for driving the phase locked loop. As noted above, Mirov fails to disclose reducing the power supplied to a PLL and therefore necessarily fails to disclose shutting off the power provided to a PLL.

In view of the foregoing, it is respectfully submitted that the anticipation rejection of claims 1-8, 13, 19, 20, 36 and 37 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejections of Claims 1-20, 24, 26-28 and 35-37

At page 4 of the Office Action, claim 14 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov and claims 1-13, 15-20, 24, 26-28 and 35-37 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann (U.S. Patent No. 5,877,656). These rejections are respectfully traversed.

Claims 2-20 depend from claim 1 and claim 37 depends from claim 36. As noted above, Mirov fails to disclose or suggest at least the limitations of disabling a phase locked loop when in a first power mode as recited by claims 1 and 36. The Office Action does not assert that Mann teaches these limitations. Accordingly, the Office Action fails to establish that the proposed combination of Mirov and Mann discloses or suggests each and every limitation of claims 1-20, 36 and 37. Moreover, the dependent claims recite additional limitations neither disclosed nor suggested by Mirov or Mann.

Claims 24, 26-28 and 35 have been canceled, thereby obviating the rejection of claims 24, 26-38 and 35.

In view of the foregoing, it is respectfully submitted that the obviousness rejections of claims 1-20, 24, 26-28 and 35-37 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Obviousness Rejections of Claims 9-12, 16-18, 25, 28, 39 and 40

At page 7 of the Office Action, claims 9-12, 16-18, 25, 28, 39 and 40 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann and further in view of Zhang (U.S. Patent No. 6,687,322). This rejection is respectfully traversed.

Claims 9-12 and 16-18 depend from claim 1 and claims 39 and 40 depend from claim 36. As noted above, Mirov and Mann fail to disclose or suggest, alone or in combination, the at least the limitations of disabling a phase locked loop when in a first power mode as recited by claims 1 and 36. With respect to claim 9, the Examiner asserts that Zhang "discloses the step of disabling the phase lock loop, when in first power mode [lower speed or PCI clock mode] . . ." *Office Action*, p. 9. However, as similarly discussed above with respect to Mirov, Zhang discloses that the PLL is merely bypassed and fails to provide any disclosure or suggestion that the PLL is disabled when in a first power mode. *See, e.g., Zhang*, col. 5, lines 19-60; *see also Id.*, col. 7, lines 12-16 (teaching that "[w]hen operating in the lower clock speed mode, on the other hand, the clock alignment and distribution devices bypasses the PLL [sic] and generates clocks with sufficient margin to accommodate the requirements of the lower clock speed)(emphasis added). Accordingly, as Mirov, Mann and Zhang fail to disclose at least the limitations of disabling a phase locked loop when in a first power mode as recited by claims 1 and 36, the proposed combination of Mirov, Mann and Zhang fails to disclose or suggest each and every limitation of claims 9-12, 16-18, 39 and 40 at least by virtue of their dependency on one of claims 1 or 36. Moreover, these claims recite additional limitations neither disclosed nor suggested by Mirov, Mann or Zhang.

Claims 25 and 28 have been canceled, thereby obviating the rejection of claims 25 and 28.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 9-12, 16-18, 25, 28, 39 and 40 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 29-33

At page 10 of the Office Action, claims 29-33 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann and Zhang and further in view of Durham (U.S. Patent No. 6,785,826).[1] Claims 29-33 have been canceled, thereby obviating this rejection. Withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 21, 22, 41 and 43

At page 11 of the Office Action, claims 21, 22, 41 and 43 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann and Zhang and further in view of Durham. This rejection is respectfully traversed.

Claims 21 and 22 depend from claim 1 and claims 41 and 43 depend from claim 36. As noted above, neither Mirov, Mann, nor Zhang disclose or suggest at least the limitations of disabling a phase locked loop when in a first power mode as recited by claims 1 and 36. The Office Action does not assert that these limitations are disclosed or suggested by Durham. Accordingly, the Office Action fails to establish that the proposed combination of Mirov, Mann, Zhang and Durham discloses or suggests each and every limitation of claims 21, 22, 41 or 43 at least by virtue of their dependency from one of claims 1 or 36. Moreover, these claims recite additional limitations neither disclosed nor suggested by Mirov, Mann, Zhang or Durham.

To illustrate, claim 21 recites the additional limitations of wherein determining a power mode includes identifying types of pending instructions and claim 41 recites similar limitations. With respect to these limitations, the Examiner asserts that Durham teaches a "method and apparatus with [a] low power mode identifying circuit (determining low power mode) including [a] power audit and control circuit for monitoring power dissipation of [a] functional unit within [a] processor. The low power mode circuit (234) examines the low power mode enable signal, the request signal and determine[s] the best time to enter the low power mode depending on types and number of pending operations or instructions to be performed by the functional unit

[1] The Office Action and attached PTO-892 incorrectly cite Durham as U.S. Patent No. 6,785,829. U.S. Patent No. 6,785,829 is issued to George et al. and does not appear to be relevant to the scope of the claims. Based on the name "Durham," the issue date and the Examiner's discussion of the disclosure, the Applicants have identified U.S. Patent No. 6,785,826 to Durham as being the actual patent referred to by the Examiner.

(col. 6, lines 41-67, col. 7, lines 1-16, col. 2, lines 4-35, col. 3, lines 26-67, col. 4, lines 1-24)." *Office Action*, p. 12. The Applicants agree with the Examiner that Durham discloses a method and apparatus for monitoring power dissipation of functional units within a processor. However, the Applicants disagree with the Examiner's assertion that Durham discloses that the low power circuit 234 determines "the best time to enter the low power mode depending on" the number of pending operations. As provided by Durham:

> If the low power mode enable signal 310 is enabled, the low power mode circuit 234 additionally examines, at a step 714, the type of operations or instructions currently being performed, or to be performed, by the functional unit 206. If they are of the type determined to be operable by the functional unit 206 in a low power mode, the functional unit 206 is placed in the low power mode 704. If not, the functional unit 206 is operated in the normal power mode 702. This approach permits more autonomy for the functional unit 206. The low power mode circuit 234 determines the best time to enter the low power mode based on ongoing internal operations, pending instructions, etc. This approach increases unit throughput.

Durham, col. 7, lines 4-16 (emphasis added).

As the above-cited passage illustrates, Durham provides that only the type of instruction is examined to determine whether or not a functional unit 206 is to be placed in a low power mode and provides no disclosure or suggestion that the number of pending instructions are considered. Accordingly, Durham fails to disclose or suggest the limitations of wherein determining a power mode includes identifying types of pending instructions as recited by claims 21 and 41.

In view of the foregoing, it is respectfully submitted that the obviousness rejection of claims 21, 22, 41 and 43 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 23, 34 and 42

At page 13 of the Office Action, claims 23, 34 and 42 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Mirov in view of Mann and further in view of Anwyl (U.S. Patent No. 5,576,738). These rejections are respectfully traversed.

Claims 23 and 42 depend from claims 1 and 36, respectively. As noted above, Mirov and Mann fail to disclose or suggest at least the limitations of disabling a phase locked loop when in a first power mode as recited by claims 1 and 36. The Office Action does not assert that Anwyl teaches these limitations. Accordingly, the Office Action fails to establish that the proposed combination of Mirov, Mann and Anwyl discloses or suggests each and every limitation of claims 23 and 42 at least by virtue of their dependency from claims 1 and 36, respectively. Moreover, these claims recite additional limitations neither disclosed nor suggested by Mirov, Mann or Anwyl.

Claim 34 has been canceled, thereby obviating the rejection of claim 34.

In view of the foregoing, it is respectfully submitted that the obviousness rejections of claims 23, 34 and 42 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Addition of Claims 44-54

Claims 44-54 have been added. New claim 44, from which claims 45-54 depend, recites the limitations of: a phase locked loop having a first input to receive a first clock signal and a first output to provide a second clock signal, wherein the second clock signal is based on the first clock signal; a first multiplexer having a first input coupled to the first input of the phase locked loop, a second input coupled to the first output of the phase locked loop and an output, wherein the first multiplexer is operable to selectively provide to the output a signal received at the first input when in a first power mode or a signal received at the second input when in a second power mode; and means for disabling the phase locked loop when in the first power mode. As established above, none of the cited references disclose or suggest the disabling of a phase locked loop when in a first power mode. Accordingly, none of the cited references disclose or suggest, alone or in combination, at least the limitations of means for disabling a phase locked loop when in a first power mode as recited by new claim 44. The cited references therefore fail to disclose or suggest each and every limitation of claim 44, as well as new claims 45-54 at least by virtue of their dependency from claim 44. Moreover, these dependent claims recite additional limitations neither disclosed nor suggested by the cited references.

Conclusion

It is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-0441.

Respectfully submitted,

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Date

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